International Journal of Electrical, Electronics and Computer Engineering 1(2): 1-5(2012)
ISSN No. (Online) : 2277-2626
Special Edition for Best Papers of Michael Faraday IET India Summit-2012, MFIIS-12

Application Specific Integrated Transducer Interface Module - Control Architecture for DC-DC Converters

J. Kamala and B. Umamaheswari***
**Department of ECE, College of Engg. Guindy, Anna University, Chennai, India*
***Department of EEE, College of Engg. Guindy, Anna University, Chennai, India*

(Received 15 October, 2012 Accepted 01 December, 2012)

ABSTRACT: This paper presents the design issues in the implementation of Application Specific Integrated Transducer Interface Module-Control Architecture (AS ITIM–CA). The architecture is capable of generating Electronic Data Sheet for transducers including system details. Controller and other functional modules are configured in adaptation to system specifications. Features of the architecture are illustrated through an application to a class of DC-DC converter systems. It suits to industrial environment because of its self descriptive nature and universal configurability. The architecture is synthesized and realized using FPGA. Advantages of this architecture are demonstrated in comparison with other existing control architectures.

Key words— Atlys Spartan 6 FPGA, DC-DC converter, Hardware Implementation, Smart transducer, Synthesis Report.

I. INTRODUCTION

Networking of transducers with controllers is used for most of industrial and medical applications [1], [2]. From 1994, there has been a lot of emphasis on usage of common communication interface for transducers [3], [4]. NIST and IEEE have formulated the universal standard called IEEE 1451 for smart transducer interface [5]. Special functions required for smart transducers are being presented by [6], [7], [8]. The protocol includes the standard for the following

1. TIM – Transducer Interface Module includes the hardware and interface required to connect the transducer with digital system.
2. TEDS – Data sheet of transducers stored electronically in a set of memory locations called TEDS (Transducer Electronic Data Sheet).

Various digital platforms such as micro-controllers, micro-processors, digital signal processors and FPGA (Field Programmable Gate Array) are used to configure the smart transducer with its functional modules [9-10]. Controller is normally configured in general way as they serve a specific purpose. The major advantage of smart transducers is the universal accessibility and effective reusability. Such smart feature of the transducer is extended to controller. Based on interconnection between transducers and control structures, various control configurations can be obtained. Existing controller configurations can be categorized into two groups, namely

1. Conventional control structure, where the transducers are dedicated part of control structure as shown in figure 1.

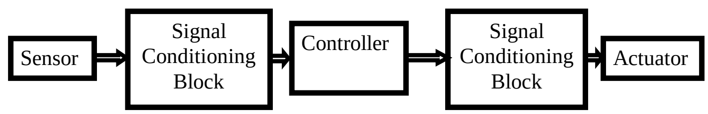

Fig. 1. Conventional control architecture.

2. TIM-based control structure, where transducer TIM and controller act independently as shown in figure 2. IEEE 1451 compliant networks have been developed to achieve inter-operability between networks, auto-discovery / configuration and dynamic adaptation to various transducers. [11-12].

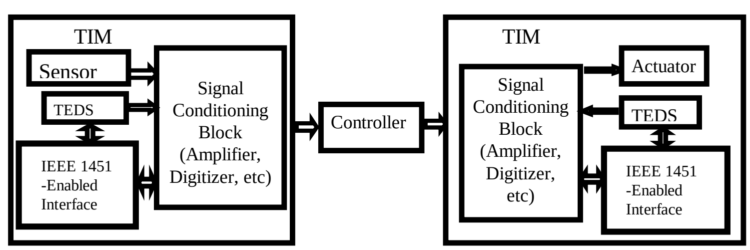

Fig. 2. TIM based control structure [13], [14].

It is attempted to integrate the controller as part of smart transducer leading to a novel architecture namely, Integrated-TIM-Control Architecture. It is designed for specific purpose as shown in figure 3.

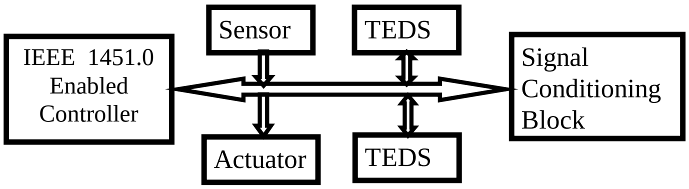

Fig. 3. Application Specific Integrated TIM-Control Architecture – AS ITIM CA.

Special purpose regulating PWM modulators like SG3524 [15], provide the switching and regulating control functions for the DC-DC converters. Combining the advantages of the IEEE 1451 protocol and special functions like regulating PWM modulators, an AS ITIM-CA is proposed. This paper illustrates the Hardware Implementation of the IEEE 1451.0 Enabled architecture in the FPGA platform.

The paper is organized with the following sections. Section II discusses the functional blocks of the architecture. Hardware implementation and synthesis report is given in section III. Validation of its functionalities is achieved by simulation results in section IV. Section V concludes with the features of the proposed design.

II. AS ITIM-CA FOR DC-DC CONVERTER SYSTEMS

A. DC-DC Converter in the TIM Perspective

DC-DC Converters change input DC voltage into different DC voltage at output. Major components of DC-DC converter system are divided into two groups as in Table I.

TABLE I COMPONENTS OF DC-DC CONVERTER

Transducer Elements	Current/Voltage sensor, temperature sensor switching device, driver, Freewheeling Diode, Snubber circuit
Other Elements	Inductors and Capacitors, Current / Voltage mode control, PID Controller, Estimator based controller

Different interconnection patterns between components lead to three configurations of converter, namely Buck, Boost and Buck-Boost converter. Output voltage variation is achieved by varying the switching frequency of converter. Hence a general structure can be defined to describe DC-DC converter system in IEEE 1451.0 format.

B. TEDS for DC-DC Converters

Table II gives the list of transducer TEDS to be formed for DC-DC converter. As per the IEEE 1451.0 standard, the first mandatory TEDS is ‘Meta TEDS’, which is defined for the system. The architecture utilizes two optional TEDS along with three mandatory TEDS for each of the transducer (sensor/actuator). Total memory requirement for TEDS storage is 7496 bits for voltage, current and temperature sensor with one actuator.

C. AS ITIM-CA STRUCTURE OF DC-DC CONVERTER

TIM structure is designed to receive IEEE 1451.0 service commands / system specifications. Sensor outputs, actuator commands and TEDS can be accessed directly by using IEEE 1451.0 service commands. It also generates TEDS from the received information. Processing module utilizes the TEDS information to provide necessary control input to system. The major functional blocks of the proposed architecture are shown in Figure 4.

TABLE II FORMATION OF TEDS

TEDS Generation	**Name, Category and Contents of TEDS**	
TIM Structure Defined for TIM	**Mandatory :-** **Meta TEDS** - Number of transducers used and other details	
Actuator 1…n Defined for each controlled switching device	**Mandatory**	**TEDS chosen from optional list**
	1. **Transducer Channel TEDS** : Signal conditioning requirement, upper, lower limit and error in sensor/actuator 2. **User Transducer Channel TEDS** : Name of sensor/actuator 3. **Physical TEDS** : Physical communication media	4. Controller order and coefficients 5. Calibration information
Sensor 1 Voltage sensor		4. System order and coefficients 5. Calibration information
Sensor 2 Current Sensor		4. Estimator order and coefficients 5. Calibration information
Sensor 3 Temperature sensor		4. Estimator based Controller order and coefficients 5. Calibration information
Total number of TEDS required = 1+5n+(3X5)		

4. End User Application Specific TEDS **5. Calibration TEDS**

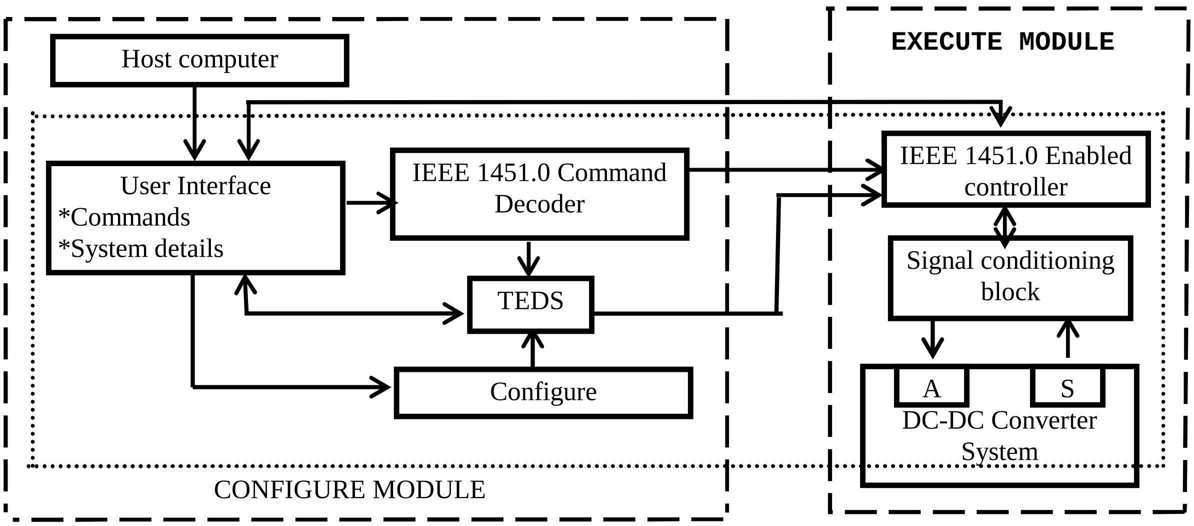

Fig. 4. Block diagram of AS ITIM-CA architecture.

The architecture basically contains 2 major functional modules namely

1. Configure module - Various parameters of functional blocks are defined and TEDS information is generated accordingly. Based on the type of converter, predefined controller structure is chosen. Enabling of controller is done in 'Execute mode'.
2. Execute module - Generates the control command, using the IEEE 1451.0 enabled controller block. Configuration of controller includes selection of suitable input/output data rates, controller parameters and switching frequency

Common functions supported by the architecture are as follows

- Formation of TEDS from the specifications of the system.
- Dynamic configuration of the functional modules of TIM
- Generation of IEEE 1451 control commands to be used by in-built controller.
- Generation of control command according to circuit configuration and user specifications.

III. Hardware Implementation Using FPGA

FPGA allow configurable architecture with more number of input / output interfaces. Hence FPGA platform is chosen to implement the architecture. External system inputs such as component values and transducer details, are received in parallel, whereas, access of IEEE 1451.0 commands and TEDS is done serially. The system requires 80 input pins and 2 output pins.

Atlys Spartan 6 FPGA is used for this application. The control command is derived from error signal, using Equation 1, where e(n) is error signal, u(n) is converter output and y(n) is duty cycle of PWM signal. Simple PI controller is chosen as per the user choice of voltage mode control of Buck converter. Controller coefficients are a1, a2 and b1, derived from End User Application Specific TEDS.

$$e(n) = u(n) - ref \qquad (1)$$
$$y(n) = a1e(n) + a2e(n-1) + b1y(n-1)$$

Hardware utilization of the FPGA i.e. the synthesis report generated by the Xilinx software is provided in Table III.

Table III : Device Utilization Summary

Logic utilization	Used	Available	Utilization
Number of slices	14392	54576	25%
Number of slice LUTs	8186	27288	30%
Number of 4 i/p LUT-FF pairs	131	351	37%
Number of DSP48A1s	4	58	6%

IV. Experimental and Simulation Results

Functionalities of the architecture are verified in both operating modes. It is simulated for various IEEE 1451.0 service commands such as accessing TEDS and registers in 'configure mode'. Execution of command is performed after receiving 56 bits of command (with offset field = 0) in the signal 'din' serial input line. Figure 5 shows the contents of various TEDS formed in the configure mode. Signals of

interest are shown in the diagram. Command 'Clear Status Event Register' execution, clears the status register and it is shown in Figure 6.

TEDS

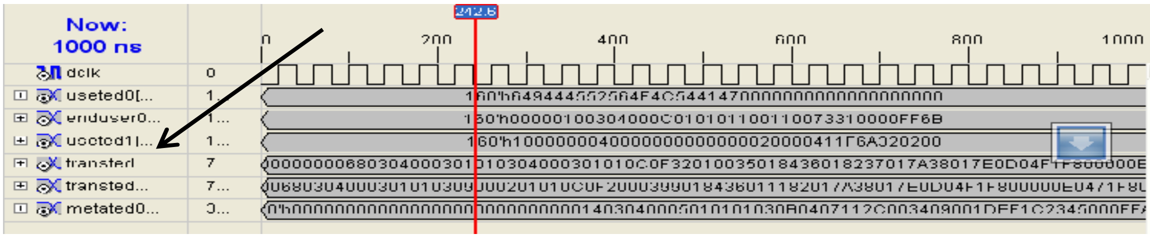

Fig. 5. Contents of TEDS.

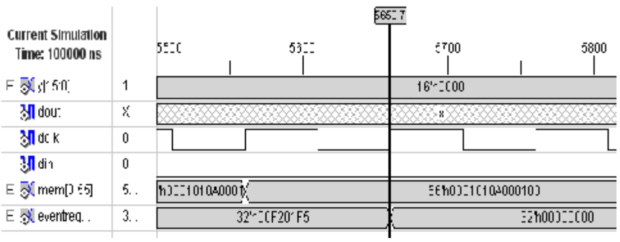

Fig. 6. Execution of the command ‘Clear Stauts Register’.

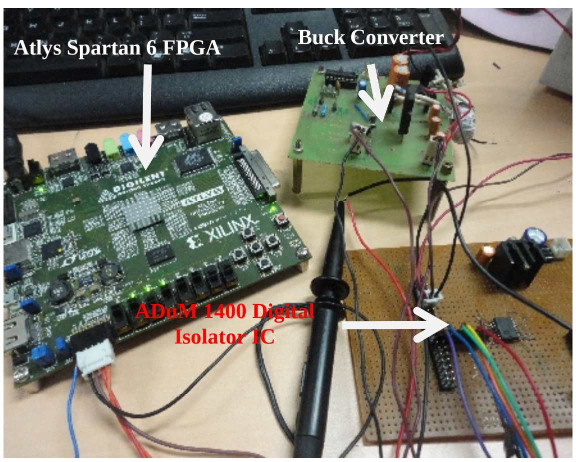

Fig. 7. Experimental Set up.

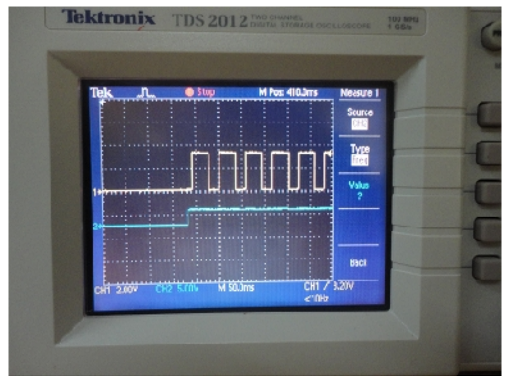

Fig. 8. PWM signal and ‘mode’ input.

Real time control command is generated for DC-DC converter in ‘Execute mode’. Control command is in the form of PWM signal applied to switching device (actuator) of DC-DC converter. Experimental set up is shown in Figure 7. Controller operation is verified by the PWM signal and converter output. Figure 8 shows the PWM signal with ‘mode’ input. PWM signal is generated only if ‘Mode’ input is applied with high level signal.

V. Conclusion

Three types of control structures namely conventional, TIM based controllers and AS ITIM-CA are compared. Conventional controllers are simple to design, but do not allow self descriptive and universal configurable structure. TIM based controller is modular and universal in its structure. In case of multi-sensor system, interdependent and redundant information is not effectively utilized by TIM based controller. AS ITIM-CA implemented in this paper can configure itself, for all types of converters and allow access of TEDS in IEEE 1451.0 format. Proposal of such architectures allow reuse and re-configurability of controllers for various applications including different transducer choices. Hardware utilization is lower for AS ITIM-CA comparing with TIM based controller. Implementation of the controller is demonstrated in real time for buck converter. The AS ITIM-CA architecture is the most preferred application, in the industry environment for its self descriptive nature.

ACKNOWLEDGMENT

Authors of this paper would like to thank for the funding provided by the Centre for Technology Development and Transfer, Research Support Scheme of Anna University, Chennai.

REFERENCES

[1] V.R. Singh and Kanika Singh, “Wireless Sensor Networks for Bio-Medical Applications in Cancer Hyperthermia”, *30th Annual International IEEE EMBS Conference Vancouver*, pp. 5160-5163, British Columbia, Canada, August 20-24, 2008.

[2] Harish Ramamurthy, Prabhu B.S, Rajit Gadth and Madni M, "Smart Sensor Platform for Industrial Monitoring and Control", *Proc. IEEE Sensors 2005, Irvine, CA.* Oct. 30-Nov.3, pp. 1116-1119, 2005.

[3] Bill Travis "Smart-sensor standard will ease networking woes", EDN, Cahners Publishing, pp. 49-55, June 22,

[4] -86, June 22, 1999

[5] IEEE Standard for a Smart Transducer Interface for Sensors and Actuators – Common Functions, Communication Protocols, and Transducer Electronic Data Sheet (TEDS) 1995

[6] Bill Travis "Sensors smarten up", EDN, Cahners Publishing, pp. 76Formats, *IEEE Standard* 1451.0-2007.

[7] Bissi, L., Scorzoni, A., Placidi, P., Marrocchi, L., Bennati, M., Zampolli, S., Masini, L., Elmi, I. and Cardinali, G. C. "A Low-cost Distributed Measurement System based on Gas Smart Sensors for Environmental Monitoring", *1st International Conference on Sensing Technology*, pp. 301-306, 2005.

[8] Rossi, S. R., Aparcido, A.de Carvaho., Da Silva, A. C. R., Batista, E. R., Kitano, C., Filho T. A. S. and Prado T. A., "Open and Standardized Resources for Smart Transducer Networking", *IEEE Transactions on Instrumentation and Measurement*, Vol. **58**, No.10, pp. 3754-3761, Oct. 2009.

[9] Wei Xue, Ying-qing Guo and Xiao-dong Zhang, "A Bank of Kalman Filters and a Robust Kalman Filter Applied in Fault Diagnosis of Aircraft Engine Sensor/Actuator", 2007

[10] Kyung Chang Lee, Man Ho Kim, Suk Lee, and Hong HeeLee, " *IEEE-1451-Based smart Module for In-*vehicle Networking Systems of Intelligent Vehicles", *IEEE Transactions on Industrial Electronics*, Vol. **51**, No. 6, pp. 1150-1158, Dec. 2004.

[11] Nihal Kularatna, B.H. Sudantha, "An Environmental air Pollution Monitoring System Based on the IEEE 1451 Standard for Low Cost Requirements", *IEEE Sensors Journal*, Vol. **8**, no. 4, pp. 415-422, Apr.2008

[12] Jorge E. Higuera, and Jose Polo, "IEEE 1451 Standard in 6LoWPAN Sensor Networks Using a Compact Physical-Layer Transducer Electronic Datasheet", *IEEE Transactions on Instrumentation and Measurement*, Vol. **60**, No.8, pp. 2751-2758, Aug. 2011.

[13] Alvaro Reina Nieves, Natividad Martinez Madrid, Ralf Seepold, Jesus Murgoitio Larrauri, and Benat Arejita Larrinaga, "A UPnP Service to Control and Manage IEEE 1451 Transducers in Control Networks", *IEEE Transactions on Instrumentation and Measurement*, Vol. **61**, No.3, pp. 791-800, Mar. 2012

[14] Kyung Chang Lee, Man Ho Kim, Suk Lee, and Hong HeeLee, " IEEE-1451-Based smart Module for In-vehicle Networking Systems of Intelligent Vehicles", *IEEE Transactions on Industrial Electronics*, Vol. **51**, No. 6, pp. 1150-1158, Dec. 2004.

[15] Anuj Kumar, I. P. Singh, and S. K. Sud, "Energy Efficient and Low-Cost Indoor Environment Monitoring System Based on the IEEE 1451 Standard", *IEEE Sensors Journal*, Vol. **11**, No. 10, pp. – 2598-2610, October 2011.

[16] ST Datasheet SG3524 : Regulating Pulse Width Modulators ST Microelectroelectronics [Online] Available : www.st.com